In the outstanding Office Action, Claim 13 was rejected under the second paragraph of 35 U.S.C. §112 because of being of similar scope to Claim 12 and Claims 9-15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sun (U.S. Patent No. 5,496,764) in view of the Wolf et al article ("Silicon Processing for the VLSI era", hereinafter Wolf) or Moon et al (U.S. Patent No. 5,985,735 hereinafter Moon) in view of Sun.

Initially, it is believed that the rejection of Claim 13 as being of similar scope to that of Claim 12 is moot in view of the cancellation of these claims.

Before considering the 35 U.S.C. §103 rejections, it is believed that a brief review of the present invention would be helpful. In this respect, Applicants' invention is directed to a method of manufacturing a semiconductor substrate having shallow trench isolation (STI) regions delineating a geometrical pattern of very small feature sizes (such as sub-micrometer sizes) at a top surface of a device region surrounded by the STI regions forming window portions without generating significant crystalline defects in the device region. The main electrode regions, such as the source/drain regions of an MOS transistor, are selectively formed by diffusing impurity atoms (or by implanting impurity ions) through these window portions.

One aspect of the present inventive method includes the steps of forming a plurality of grooves on part of a surface of the semiconductor substrate, depositing oxide films in the grooves by an organic silicon based CVD method, removing an upper part of the oxide film so as to planarize a surface of a resultant structure until a surface of the semiconductor substrate is substantially exposed (note the specification at page 11, lines 6-26, for example), and annealing the oxide films at a substrate temperature of 1100 to 1350°C so as to avoid generating significant crystalline defects. The portion of the semiconductor substrate

exposed by the planarizing step serves as "a top surface of the device region" which corresponds to the window portions through which the main electrode regions of semiconductor active elements can be formed.

In a further aspect of the present invention, the grooves each have a depth d and a width 1_{1x} so as to provide an aspect ratio $d/1_{1x}$ less than 10 and a line-and-space ratio $1_{1x}/1_{2x}$ less than 1.5, wherein 1_{2x} is a space between the grooves measured along the same x direction used to measure the groove width. With these very fine geometrical dimensions and a configuration having such a high aspect ratio, only buried oxide films formed by the claimed organic silicon based CVD method can provide the crystallographic quality such that the dislocation density generated in the semiconductor substrate in the vicinity of the grooves is less than $1/\mu m^2$ (note, for example, Fig. 4 and the description at page 11, lines 5-36 as well as at page 20, line 33 to page 21, line 4). It is well known in the art, that a thermal oxide film cannot achieve such small geometrical dimensions with such a high aspect ratio.

In addition, while conventional oxide films deposited by organic silicon based CVD methods include low temperature processing for achieving small geometrical dimensions and a high aspect ratio, they do not provide the above noted superior crystallographic structure in terms of the above-noted dislocation density. The conventional films with poor crystallographic structure and higher dislocation densities inherently lead to internal stress which generates large and high density crystalline defects in the semiconductor substrate formed as the device region sandwiched by the grooves. Note, Fig. 2, for example. The stress due to shrinkage caused by dissociation of moisture that is inherently contained in the present day organic silicon source material is what generates many crystalline defects, such as dislocations in the semiconductor substrate.

On the other hand, with the claimed annealing step of the oxide films at the claimed substrate temperature of 1100 to 1340°C, the oxide film is provided containing a "predetermined rate" of higher order ring structures and a "predetermined rate" of lower order ring structures (see Fig. 7A, for example), and stress in the buried oxide films is relaxed. Therefore, the generation of crystalline defects in the semiconductor substrate is suppressed as shown in Fig. 11, for example, and the dislocation density in a vicinity of the groove becomes less than $1/\mu m^2$ as noted at page 20, lines 33-36 of the specification, for example.,

Further, the annealed oxide film, which is annealed at the claimed substrate temperature of 1100 to 1350°C, provides an etching rate with ammonium fluoride (NH_4F) solution that is about 130 mn/min and close to the etching rate of a thermal oxide film (see, for example, Fig. 7B and the description at page 22, line 34 to page 23, line 9).

Therefore, providing a semiconductor substrate having the claimed geometry of oxide filled isolation grooves around device regions that are annealed at the claimed substrate temperatures provides the advantage of a lower dislocation density and a lower leakage current even with a high packing density being used.

Turning now to Sun, there is no disclosure or suggestion of the claimed step of removing the upper part of the oxide film so as to planarize the surface of the resultant structure until the surface of the semiconductor substrate is substantially exposed with the exposed semiconductor substrate serving as a top surface of a corresponding device region through which the main electrode regions of semiconductor active element can be formed. As shown in Figs. 4-8, Sun discloses the method for bonding substrates 10 and 20 together (see col. 3, lines 13-27). To do this, the exposed surface of the substrate 20 is polished by an oxide polishing step (see col. 2, lines 57-62), so it can serve as the bonding surface to be

mated with substrate 10 through the thin oxide layer 61. Fig. 8 of Sun clearly shows that the surface exposed by the oxide polishing step serves as "the bottom surface" of the device region, not the top surface that Claims 9, 25, and 29 require.

Although the action contends that col. 3, lines 13-27 teaches annealing the substrate at a temperature of 1000 to 1200°C, col. 3, lines 13-27 actually teach that bonding of two substrates is performed at a temperature of 1000 to 1200°C. Thus, Sun fails to show the third step of Claim 9 requiring the annealing of the oxide films at the substrate temperature of 1100 to 1350°C so that dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than $1/\mu m^2$. In view of the presence of film 61 as well as substrate 10 and insulating layer 11 of Sun, which are required for bonding, there will clearly be differences in crystallographic structure and dislocation density. Thus, the invention of Claim 9 is clearly not taught or suggested by Sun any more than the inventions of Claims 25-29 are.

Sun also fails to teach or suggest an organic silicon based CVD method. In this respect, the Action proposed the combination of Wolf and Sun. However, the proposed combination of Wolf and Sun does not cure the deficiencies in Sun, since in Wolf there is no disclosure or suggestion of the claimed annealing step for alleviating crystallographic stress so as to obtain the claimed low dislocation density of less than $1/\mu m^2$. Accordingly, although a description relating to a CVD method employing TEOS can be found at table 4, page 194, this suggestion is totally unrelated to any processing to alleviate crystallographic stress. Moreover, the problem of providing conformal films argued at page 3, lines 8-10 of the Action as demonstrating motivation as to forming the film 41 of Sun has no relevance to this film 41. Clearly, Sun teaches the use of a silicon dioxide insulation that overfills trenches 31. Note col. 2, lines 46-54. Thus, there is no motivation to combine Wolf and Sun because of

any need for a conformal layer.

Moon also has no disclosure or suggestion of the claimed third step of annealing the oxide films at the substrate temperature of 1100 to 1350°C, even though the Action proposes the combination of Sun and Moon. Thus, the proposed combination of Sun and Moon does not cure the deficiencies in Moon because Sun, as noted above, has no disclosure or suggestion of claimed annealing step for alleviating crystallographic stress so as to obtain the claimed low dislocation density of less than $1/\mu m^2$. Merely because Sun teaches that bonding the two substrates through layer 61 is performed at a temperature of 1000 to 1200°C (see col. 3, lines 13-27), this provides no reasonable basis to modify Moon who has no need to perform such bonding. Thus, since Sun fails to teach or suggest some reason besides the disclosed bonding of the two substrates as requiring the disclosed heating and does not teach or suggest the claimed organic silicon based CVD method, the Action fails to establish any reasonable motivation for combining reference teachings.

Moreover, as shown in Fig. 4, Moon discloses that the surface of the thermal oxide film 14 is transformed (via nitrogen plasma) into a nitrogen-rich surface 15, see col. 5, lines 52-54 and col. 6, lines 29-42. This is done so as to suppress the formation of crystal defects in the semiconductor substrate. Accordingly, it is clear that Moon employs the moderately sloped sidewall geometry of trench 13 and the nitrogen-rich surface 15 to suppress the formation of crystal defects in the semiconductor substrate, and has no reason for annealing for such suppression. Thus, there is no motivation to alleviate crystallographic stress by optimizing the annealing temperature as to the claimed temperature range of 1100 to 1350°C. In this regard, Moon teaches an absolutely different structure, that is, the triple layered structure consisting of CVD oxide layer 16, the nitrogen-rich surface 15 and the thermal

oxide film 14 and the artisan would have no reason to suspect that there is any optimum temperature range for alleviating crystallographic stress of the Moon triple layered structure (shown in Figs. 5-6) or that it would coincide with the claimed temperature range, even if he is taught by Sun to bond substrates at this temperature. Any allegation that it would be obvious to anneal the oxide films at claimed substrate temperature of 1100 to 1350°C can, thus, only be based upon a hindsight reconstruction of Moon and Sun in light of the present disclosure which is improper.

Therefore, the Examiner's rejection of Claims 9-11, 14, and 15 under 35 U.S.C. §103(a) in view of the combination of Wolf and Sun or the combination of Sun and Moon are both believed to be improper and are respectfully requested to be withdrawn.

Since no other issues are believed to be outstanding in the present application, it is believed to be clearly in condition for formal allowance and an early and favorable action to that effect is therefore respectfully requested.

Respectfully submitted,

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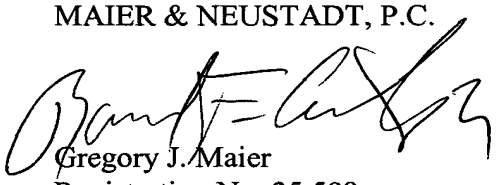
MAIER & NEUSTADT, P.C.



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16.4

An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)

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ABSTRACT

Densification methods using H_2O and N_2 ambient annealing of the filled CVD oxide for quater micron STI are compared. Although the H_2O ambient oxidation is more effective in terms of the resistance against the HF etching, volume expansion by the trench sidewall oxidation generates a large amount of stress in the narrow isolation region. However, an N_2 gas ambient annealing at high temperature shows a low stress and a low HF etch rate which enable us to fabricate the stable quater micron STI.

INTRODUCTION

As a substitute for the LOCOS isolation in sub-half micron devices, STI has been challenged widely [1,2,3]. In STI, refilling of the trenches with CVD oxide using TEOS based APCVD or LPCVD have been considered as appropriate methods due to their good filling capability without forming voids. However, those CVD oxides initially have a very high etch rate in an HF solution. Proper densification, therefore, is required for the decrease in consumption of the oxide by subsequent process steps. Annealing in an H_2O ambient is known to be one of the most effective densification methods [4]. Figure 1 shows the comparison of the final profiles of the STI with and without H_2O densification.

However, a densification in the oxidizing ambient causes an unwanted sidewall oxidation, which in turn exerts an extreme stress toward the active Si area of the devices. The stress, if it surpasses the yield stress of the Si, may form crystallographic defects such as dislocations which increase the leakage current of the STI.

In this paper, the influence of the densification in the oxidizing (H_2O) and the inert gas (N_2) ambient was being compared, and the process condition for the quarter micron STI was optimized.

EXPERIMENTAL

Test structures for isolation profile observation and electrical properties were made as shown in fig.2. At first, field and active region were defined by photolithography and etch steps (fig.2 (a)). Trench sidewall oxide was grown, CVD oxide was deposited to fill the trenches (fig.2 (b)), and two densification processes were performed seperately. CMP was then applied to planarize the CVD oxide until SiN was exposed (fig.2 (c)). SiN layer was subsequently removed in phosphoric acid, and channel stop implantation was carried out. Then, the pad oxide was removed in a diluted HF solution (fig.2 (d)). Afterwards, conventional processes were performed and the junction and transistor characteristics were evaluated.

RESULTS AND DISCUSSION

Figure 3 shows the N^+/P junction leakage currents in the H_2O densification cases. At the large isolation sizes, a normal behavior with low leakage currents is obtained, but as the isolation size becomes smaller, leakage currents in low voltages begin to increase to 80 pA/cm at 4 V in 0.26 μm isolation size. Secco etching [5] of the active and field array reveals the defects with a very high density in the narrow STI, meanwhile no defects in the wide STI as shown in fig.4 are observed. This size dependency can be explained by assuming the field oxide as a visco-elastic medium. In the case of the wide field area, the field oxide is wide enough to absorb the stress caused by the areal expansion, whereas in the narrow field area, the oxide cannot hold the stress in itself and the defects are generated to release the stress.

On the other hand, fig.5 and fig.6 show the results of the CVD oxide densification in an N_2 ambient. Figure 5 shows no increase of the leakage current in the narrow field area, which means that the leakage current has no size dependency since no sidewall oxidation occurs. These clean electrical data correlate well with the Secco observations which show no defects regardless of the isolation size [fig.6]. SUPREM-IV simulations (fig.7) also verify the stress level reduction with N_2 ambient annealing.

Figure 8 compares the $Id\text{-}V_g$ characteristics of the transistors with three different densifications. Unlike the ones with wet oxidation and N_2 ambient at 1150 °C, devices with 1000 °C, N_2 ambient densification show hump characteristic in transistors. That is because in the 1000 °C, N_2 anneal case, the top portion of the Si trench edges (fig.10 (b)) are exposed to the high electric field of the gate during HF etch steps subsequent to the densification due to the relatively high HF etch rates of the oxides (fig.9). Meanwhile, the top corners of the Si trench are mostly covered with the CVD oxide, which prevents them from being easily inverted by the electric field of the gate both in the case of the wet oxidation and N_2 anneal at 1150 °C (fig.1 (a) and fig.10 (a)), and consequently demonstrate good transistor characteristics (fig.8).

Fully working samples of the 256 Mbit DRAM were obtained by applying the STI process with the densification in an N_2 ambient at 1150 °C.

CONCLUSION

We have compared the isolation and MOS device characteristics of the STI fabricated by the densifications of the field CVD oxide in the H_2O and N_2 ambient. In H_2O ambient, the trench sidewall oxidation generates defects at the narrow trench resulting in leaky isolation characteristics. The annealing in the N_2 ambient at 1150 °C densifies the CVD oxide efficiently without causing any abnormalities in the isolation and the MOS device characteristics.

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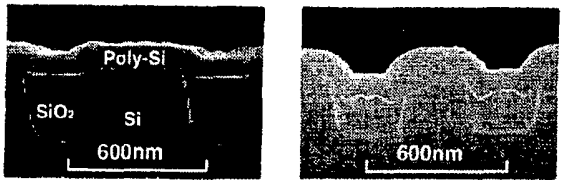


(a) (b)

Figure 1. Cross-sectional SEM micrographs of the final STI profiles (a) with and (b) without the densification. Densification was performed in H_2O ambient at 850 ℃, 30 minutes.

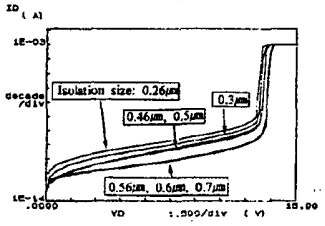


Figure 3. Junction leakage currents of the N+/P junction with respect to the reverse bias voltages. Peripheral length was 5.04 mm and the densification was done in H_2O ambient at 850 ℃, 30 minutes.

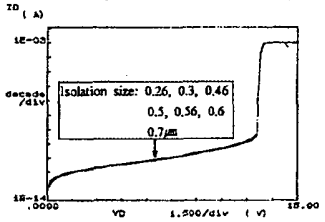
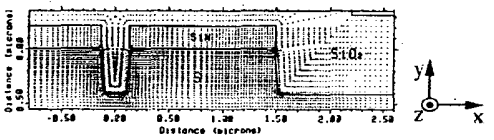
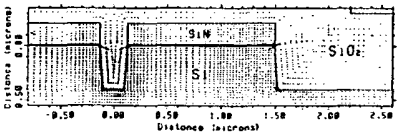


Figure 5. Junction leakage currents of the N+/P junction with respect to the reverse bias voltages. In this case, densification was performed in N_2 ambient at 1150 ℃, 1 hour.



(a)CVD Oxide Densification Condition: H_2O Ambient, 850 ℃, 30min



(b)CVD Oxide Densification Condition: N_2 Ambient, 1150 ℃, 1 hour

Figure 7. Stress simulations with SUPREM-IV(σ_{xx}). The darker area represents where the stress is more concentrated.

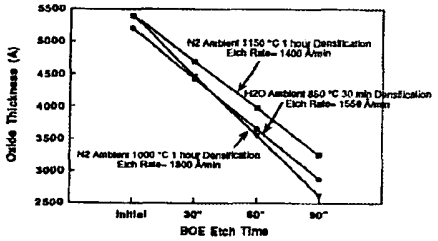


Figure 9. CVD oxide thicknesses as a function of the Bufferd Oxide Etchant (BOE) etch time in different densification conditions.

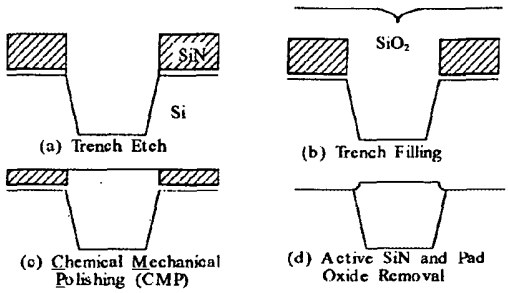
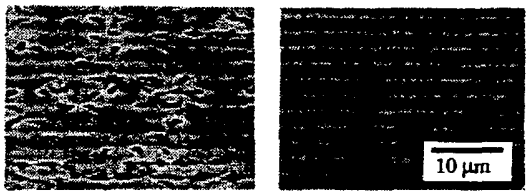
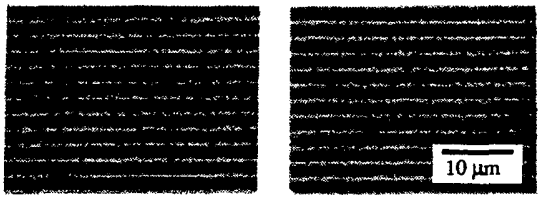


Figure 2. STI process.



(a) 0.26 μm (b) 0.7 μm

Figure 4. SEM micrographs of the Secco etched active and isolation lines. No defect is shown at wide isolation sizes whereas many etch pits which were generated by the stress in Si substrates are shown at small isolation sizes.



(a) 0.26 μm (b) 0.7 μm

Figure 6. SEM micrographs of the Secco etched active and isolation lines. No defect is shown.

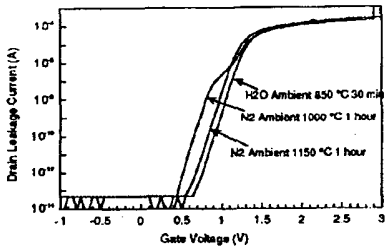
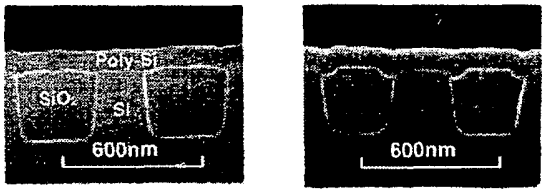


Figure 8. I_d-V_g characteristics of NMOS transistors with N_2 or H_2O ambient densification. V_d=0.1 V, V_{sub}= -3 V, W=10 μm, and L= 1.0 μm.



(a) N_2 Ambient, 1150 ℃ 1 hour (b) N_2 Ambient, 1000 ℃ 1 hour

Figure 10. Cross-sectional SEM micrograph of the final STI profile with the different CVD oxide densification conditions.